The Effect of Nonideal Polar Monolayers on Molecular Gated Transistors

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ABSTRACT Nonideal polar monolayers can induce a field-effect in molecular gated transistors. To quantify the magnitude of this phenomenon, we have calculated the effect of roughness and noncontinuity of such layers on the operation of hybrid silicon-on-insulator field-effect transistors. The results show that under most practical conditions, the nonideality of polar monolayers induces very small electric fields in the underlying transistor channel, and consequently a negligible gating effect.

KEYWORDS: nonideal polar monolayers • molecular-gated transistors • semiconductor interfaces • self-assembled monolayers • field-effect transistors

INTRODUCTION

The use of hybrid devices, in which molecular properties govern their functionality, allows us to combine the power of organic molecular synthesis (1) with the benefits of today's microelectronic technology (2, 3). For example, layers of polar organic molecules create a surface dipole with which the energy barriers at the surface or interface between two materials can be modified (4−6). Self-assembled monolayers (SAM) are also widely used as linkers between semiconductor surfaces and biological molecules in biosensors (7−9). Because of the long range of electrostatic forces, the polar monolayer electronic functionality is determined, among other factors, by the size of the molecules, layer topology, and adsorption pattern (10).

This work deals with field-effect-based chemical sensors, CHEMFETs, operating without a reference electrode; this device is sometimes also termed a molecularly controlled semiconductor resistor, MOCSER (4). Another example of such a device is shown in Figure 1 in which a molecular layer is directly adsorbed on the top dielectric of a back gated silicon-on-insulator (SOI) transistor. This layer changes the potential in the conducting channel, thus controlling the transistor current (11, 12).

It should be noted that in the absence of a reference electrode, an ideal polar layer should not induce any field in the channel, because the electric field is confined within the layer, much like in a classic infinite parallel-plate capacitor (4, 10). Nevertheless, Capua et al. have recently shown that under certain conditions polar monolayers can also change the transistor current (13). A correlation between the threshold voltage and the polarity of the functional group of molecules grafted directly on the silicon of a FET device was recently reported by He et al. (14−16). Paska et al. have shown that the field effect induced by silane monolayers can be controlled by varying the percentage of cross-linking (17).

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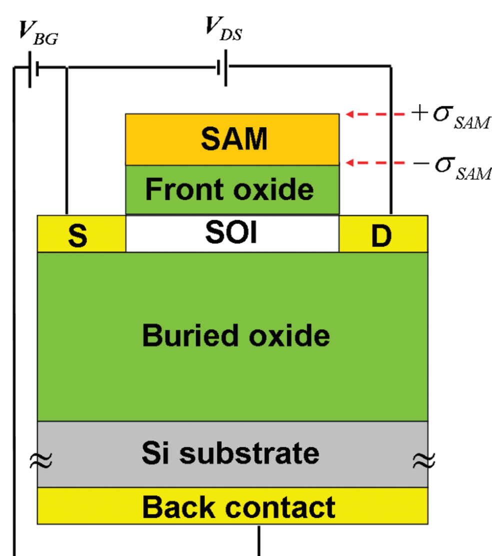

FIGURE 1. Schematic cross-section of the simulated bottom-gated SOI field-effect transistor. S and D stand for source and drain, and SOI is the low-doped silicon-on-insulator layer in which the current is conducted. A dipolar layer on top of the outer oxide layer (SAM) is modeled by two surface charge densities of opposite signs as indicated by the dashed arrows. The buried oxide layer used in the simulation was 1 μm thick, the top oxide layer was 4 nm, and the channel length was 10 μm.

Also, we have recently shown that amine-terminated self-assembled monolayers on the gate-dielectric of a device similar to the one shown in Figure 1 changes its threshold voltage (18). Considering a possible mechanism for these results, Natan et al. have estimated that fringing fields that originate from nonideal (discontinues) polar monolayers might induce a field effect that will be correlated with the net-dipole (10).

The effect of layer quality and coverage was previously studied in devices using a reference electrode in which a voltage drop is expected over the polar layer. It was shown that even partial monolayers can affect the barrier height and conductance of semiconductor surfaces (19−22). Control over the work function of silicon was demonstrated by the careful modulation of the molecular coverage (23, 24),

and the effect of coverage on impedance measurements was also analyzed (25, 26). The effect of SAM on organic FETs was recently modeled by Possanner et al. (27).

Nonideality of polar monolayers was previously suggested as one of the mechanisms for molecular gating; however, the magnitude of this effect under practical operating conditions is yet to be determined. The objective of this work is to analyze whether typical nonidealities are an important factor in transistor gating. To achieve this, we have simulated the effect of roughness and noncontinuity of such layers on the threshold-voltage of the commonly used hybrid silicon-on-insulator MOSFETs.

MODEL

The devices simulated in this work were double-gated fully depleted silicon-on-insulator (SOI) transistors, schematically shown in Figure 1 where S and D represent source and drain. The SOI layer was a 30 nm lightly doped (1×10^{15} cm^{-3}) p-type silicon, thin enough to be in the fully depleted operation mode. Consequently, the surface potentials of both SOI$-SiO_2$ interfaces (top and bottom) are coupled, which enables the study of the top interface potential using the bottom MOSFET gate as we have recently shown (13). The buried oxide (BOX) layer was 1 μm thick, the top oxide layer was 4 nm and the channel length was10 μm. A fixed interface charge $\sigma_i = 1 \times 10^{11}$ cm^{-2} was assumed at the bottom SOI$-SiO_2$ interface.

A dense dipolar SAM on top on the outer oxide layer was modeled by two parallel surface charge densities $\pm\sigma_{SAM}$ as depicted in Figure 1. The dipole moment of the molecules was assumed to be 1.5 D, the thickness of the layer 1 nm, and the molecular footprint 0.2 nm^2. Consequently, the charge density used was $\sigma_{SAM} = 1.56 \times 10^{13}$ cm^{-2}. The permittivity of SiO_2 was used as an approximation for the monolayer. Even though the permittivity of organic monolayers is usually considered to be slightly lower (~2.5) it does not significantly affect the results shown in this paper. The voltage drop over the monolayer is then calculated using the Helmholtz relation (4, 24): $\Delta\chi = (N\mu)/(\varepsilon) = 0.72$ V, where N is the molecular density, μ the dipole moment, and ε the molecular layer permittivity. Depolarization effects as discussed in refs 4 and 10 were not considered, and thus the results may be viewed as an upper limit for the molecular gating effect. The transistor with the polar monolayer on the top oxide layer, as shown in Figure 1, was simulated in two dimensions (28) using the commercial Synopsys TCAD Sentaurus semiconductor simulator. The transistor $I-V$ curves were calculated and the threshold voltage was extracted using an extrapolation of the linear region.

Discontinuity in the polar layer was modeled by an appropriate lateral gap in both surface charge densities $\pm\sigma_{SAM}$. Simulation of a polar layer, containing a single 20 nm gap (a hole), on the transistor top dielectric layer is shown in Figure 2. By examining the absolute value of the electric field (Figure 2a), it is seen that the field is confined within the two parallel surface charge densities. However, in the vicinity of the gap, the field sharply decays as a function of distance both into the dielectric and the silicon

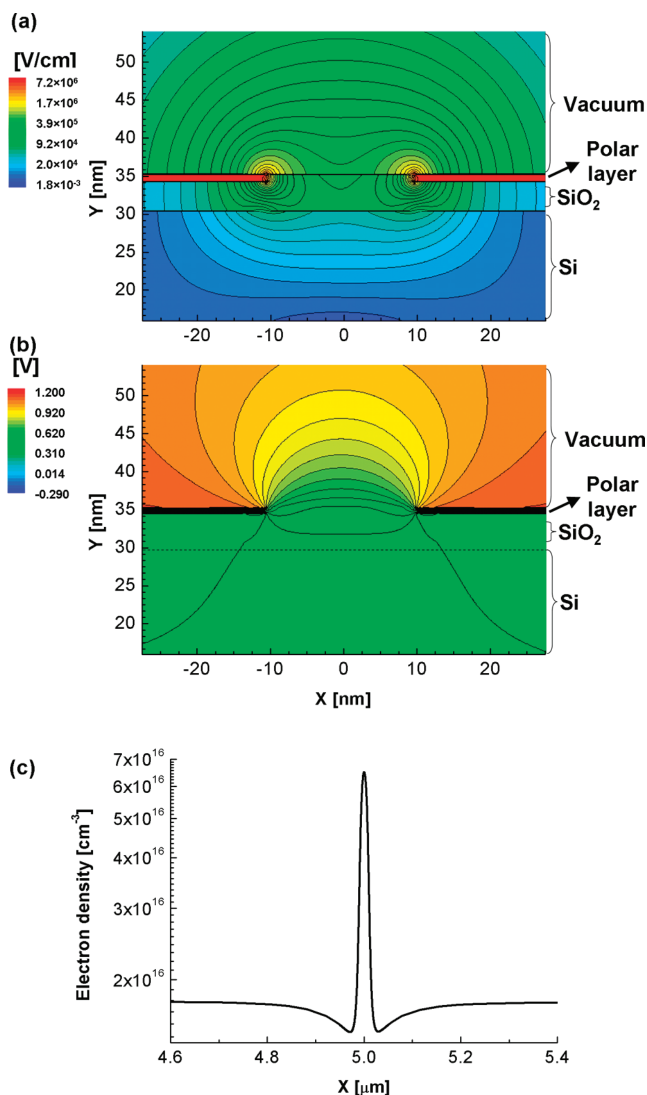

FIGURE 2. Simulation of a polar layer, containing a single 20 nm gap (a hole), on the transistor top dielectric layer. (a) Absolute value of the electric field in the vicinity of the gap is shown in an inverse hyperbolic sine scale. (b) Electrostatic potential in the vicinity of the gap. (c) Cross-section of the electron density in the SOI layer (drawn from source to drain) adjacent to the Si$-SiO_2$ interface and underneath the center of the hole.

layers; 15 nm below the gap the field is practically zero. The edges of the gap can be considered as point sources for the electric field that is not confined in the layer. Furthermore, when examining the electrostatic potential in the same area (Figure 2b), the voltage drop $\Delta\chi$, as calculated by the Helmholtz relation, is clearly observed.

It should be noted that charge transfer from the SAM to the transistor channel can take place in molecular gated transistors. However, it is not directly related to the nonideality of the layers but rather to the dipole moment. Because we quantify here the nonideality of polar monolayers, a thick dielectric layer between the molecules and the silicon channel is always assumed and charge transfer is not allowed. Nevertheless, simulation conducted for a top oxide layer thickness smaller than 4 nm (without charge transfer) yielded only slightly larger shifts in threshold voltage (up to twice as large) compared to the ones presented in the paper.

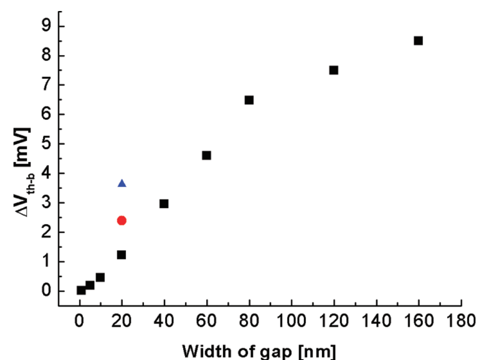

FIGURE 3. Threshold-voltage shift as a function of gap width (■). The circle (•) and triangle (▲) represent the threshold voltage shift resulting from two and three 20 nm gaps, respectively, placed far from each other.

RESULTS AND DISCUSSION

A cross-section of the electron density in the SOI layer is shown in Figure 2b; the profile is drawn from source to drain, adjacent to the top Si−SiO_2 interface, and centered underneath the gap. In this calculation the back-gate electrode was biased (1 V) to induce inversion in the SOI layer. It is observed that the electric field has a significant effect in a radius of about 0.15 μm around the gap. The field causes an increase in the electron density underneath the center of the gap, and a decrease further along the x-axis. At a distance of about 0.15 μm from the center the value of the electron density drops back to the background value (∼1.8 × 10^{16} cm^{-3}) for the applied gate bias of 1V.

Figure 3 shows the back threshold voltage shift of the transistor, ΔV_{th-b},as a function of the gap width (black squares); the threshold shift is defined relative to that of a transistor simulated with a polar layer having no gaps and using an identical finite-elements mesh. It is seen that a wider gap results in larger shifts in threshold voltage. At a certain gap width the gap edges are sufficiently apart to be considered as two separate point sources (for electric field) and therefore the ΔV_{th-b} value is expected to saturate, as seen in Figure 3 at a distance of ∼120 nm. The threshold voltage shift is positive, which means that the channel current is decreased similar to the gating effect of a negatively charged layer.

The results of similar simulations, but for two (circle) and three (triangle) 20 nm wide gaps, are also shown in Figure 3. The distance between the gaps was set to be much larger than 0.15 μm, the radius for which a single gap has a measurable effect. It is observed that the total threshold voltage shift of several gaps is a sum over the threshold voltage shifts resulting from a single gap. By using a back of an envelope calculation, for a maximal gap density (i.e., a 50% duty cycle) over the channel, (where each gap contributes ΔV_{th-b} as presented in Figure 3), we estimated the total ΔV_{th-b} to be ∼200−400 mV (29). It should be emphasized that this voltage shift is small because the back-voltage is applied through a 1 μm thick buried oxide layer, and is equivalent approximately to ∼20−40 mV front-gate threshold-voltage shift in a standard MOSFET. All the above calculations were also conducted for a transistor with 30 nm top-oxide layer, and it was found that ΔV_{th-b} was negligible.

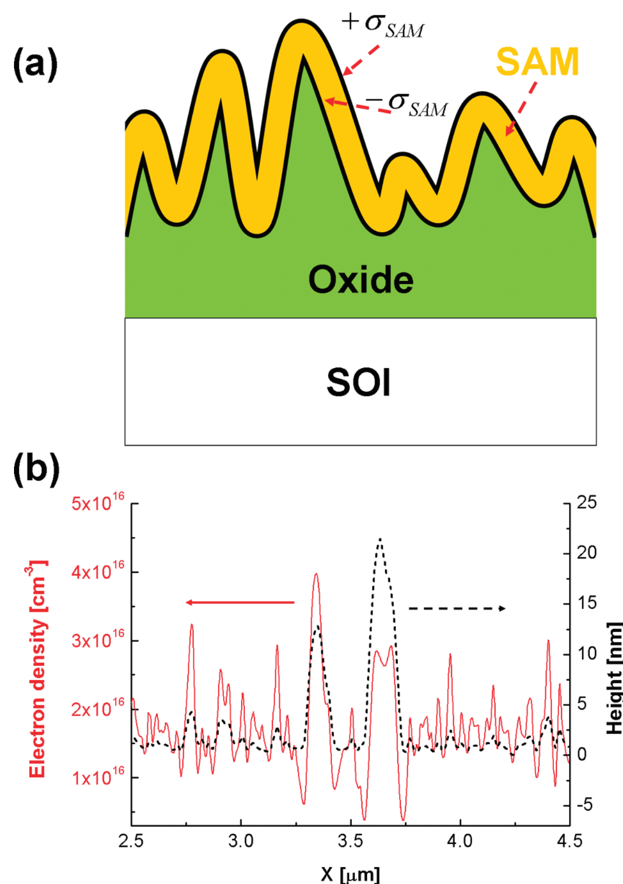

FIGURE 4. (a) Schematic cross-section of a polar layer on the rough surface of the transistor top dielectric layer. (b) Cross-section of the electron density (solid line, left axis) in the SOI layer (drawn from source to drain) adjacent to the Si−SiO_2 interface and the corresponding topography (dashed line, right axis) of the oxide layer plotted as a function of the distance from the source, and zoomed over 2 μm.

Nonideality of self-assembled monolayers can be manifested not only in partial coverage but also in the surface roughness. Consider a surface covered with positive and negative charged layers $\pm\sigma_{SAM}$ (modeling a polar molecular layer) that follow the substrate topography variations, while keeping the distance between the charges constant as shown schematically in Figure 4a. Any sharp topographic feature will violate the infinite parallel plate capacitor approximation and a field distribution that resembles that of a gap is to be expected. To examine the electrostatic effect of a typical monolayer self-assembled on a rough dielectric surface, we have calculated the threshold-voltage shift of a transistor covered by such a layer.

Figure 4b shows (dashed line) the topography profile of a 3-aminopropyltrimetoxysilane (APTMS) monolayer self-assembled on SiO_2 and measured by AFM. This organic molecule is commonly used as a linker between silicon and biomolecules, and is known to create a field effect in molecular gated transistors (12). The polar layer was modeled as described in the previous paragraph and Figure 4a, whereas the top oxide surface texture is the AFM measured APTMS profile. The solid line in Figure 4b is the resulting electron density in the SOI layer (drawn from source to drain) adjacent to the Si−SiO_2 interface plotted as a function

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of the distance from the source electrode. The background value of the electron density (∼1.8×10^{16} cm^{-3}) is the same as in Figure 2b, because the same bias was applied to the back-gate electrode (inducing inversion in the SOI layer). It is observed that each sharp topographic feature induces a local modulation of the electron density similar to the one shown in Figure 2b. The shift in back-gate threshold voltage due to only such surface roughness (30) was calculated to be around100 mV. Again, we note that all the above calculations were also conducted for a transistor with 30 nm top-oxide layer, and it was found that ΔV_{th-b} was negligible.

When comparing the results of our calculations with experimental results, it is useful to devide them into two main groups. In one, there is a direct contact between the molecular layer and the semiconductor, and thus charge transfer between them is feasible (see for example ref 31); in the second, the molecular layer and the semiconductor are separated by a relatively thick oxide layer and no charge transfer can take place.

Back threshold-voltage shifts following self-assembly of (3-aminopropyl)-trimethoxysilane polar monolayer measured on identical devices as described in this paper have been shown to be in the order of 10 V (12). When comparing this to the simulation results, for both types of nonidealities, which were less than half a volt, it can be concluded that the effect of nonideality seems to be very small. Bearing that in mind, our results can now be compared to systems in which the molecules are directly grafted on the conducting medium. He et al. have shown a back threshold shift of several volts that depended on the electron-donating ability of the grafted molecules (15). As before, the observed shifts in threshold voltage are too large to be explained by the nonideality of the polar layers and the explanation given in the paper concerning charge transfer is much more plausible. In general, apart from charge transfer, two other mechanisms might be responsible for the field effect induced by polar monolayers. The first is a change in surface or interface states distribution due to the bond formation on the SiO_2 surface (17, 32). The second mechanism is the protonation of the functional groups (where relevant, for example amine groups). It is very likely that a high percentage of the molecules are protonated; the charge will induce changes in the threshold voltage.

SUMMARY

In summary, the electrostatic effect of nonideal polar monolayers on molecular gated transistors was studied by simulating such devices with rough and noncontinuous layers. The polar monolayers were modeled as two parallel surface charge densities on the transistor top dielectric layer. The results indicate that typical imperfect monolayers induce very small electric fields in the transistor channel, which result in small shifts in the transistor threshold voltage. However, it must be noted that in the case of a very thin (or native) gate oxide layers, where charge transfer to the transistor channel is possible, the dipolar character of the self-assembled monolayers is expected to have a larger effect on the transistor channel conductivity.

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(28) The third dimension was not needed because it was found either not to affect the results or diminish them slightly (depending on the density of features in that dimension).
(29) Although the effect of each gap in a dense array is different from that in a sparse one, the difference is small. This can be demonstrated by comparing the case of three 20nm gaps to that of one 60nm gap, both yielding similar ΔV_{th-b}. The contribution of dense 20nm gaps would not exceed those values.
(30) This threshold voltage shift is relative to the shift calculated for the same topography and finite-elements mesh but without the surface charge densities.
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